REMARKS

Claims 1 - 14 are pending in the present application. By this Amendment, claims 1, 2, 4, 5 and 7 – 12 have been cancelled, claims 3, 13 and 14 have each been amended, and new claim 15 has been added. No new matter has been added. It is respectfully submitted that this Amendment is fully responsive to the Office Action dated December 23, 2004.

Allowable Subject Matter:

Applicants gratefully acknowledge the indication in item 9 of the Office Action that claims 3 and 6 would be allowable, if amended, to include all of the limitations of the base claim and any intervening claims.

It is respectfully submitted that claim 3 has been rewritten into independent to include the features of base claim 1. Thus, it is submitted that independent claim 3 is allowable and claim 6 is allowable by its dependency on claim 3.

35 U.S.C. §112, Second Paragraph Rejection:

Claims 7 - 12 stand rejected under 35 U.S.C. §112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

This rejection is respectfully traversed.

As stated above, each of claims 7 – 12 have been cancelled thereby rendering this rejection moot.

As to the Merits:

1) Concerning the technical content of the invention

The invention of the present case relates to solid-state image apparatus in which a solid-state image pickup device chip is packaged in CSP (chip size package), and relates more particularly to hermetic seal portion thereof. Amended claim 3 is an independent-form amendment of original claim 3 which has been indicated as patentable, as discussed above. Since it has connection with the inventions of other claims, its technical content will be described below.

The frame portion of a hermetic seal portion of the solid state image pickup apparatus according to amended claim 3 at least includes: a metal wiring; a bump formed on solid-state image pickup device chip and electrically connected to the metal wiring; a frame base portion having the metal wiring formed on one surface thereof and adhered at the other surface thereof to a flat plate portion; and a sealed region for sealing the periphery of the bump by a sealing.

In other words, the solid-state image apparatus according to amended claim 3 is characterized in construction of the frame portion of the hermetic seal portion so that: a hermetic seal portion with an increased strength and high reliability can be obtained; a small-size packaging is

feasible; an improved throughput is achieved; and an electrical connection with an external section is made easier.

2) The solid-state image apparatus according to amended claim 13 has a hermetic seal portion comprising: a flat-plate portion formed of a transparent member; and a frame portion at least including a metal wiring disposed on a side portion of a lower surface of the flat-plate portion, a bump formed on solid-state image pickup device chip and electrically connected to the metal wiring, and a sealed region for sealing the periphery of the bump by a sealing material; wherein a wiring region or an electrode pad region is formed from an electrode pad provided on the solid-state image pickup device chip to a side surface or through the side surface to a back surface of the solid-state image pickup device chip so that an external terminal can be electrically connected to the wiring region or the electrode pad region.

With such construction, an optimal electrical connection structure to an external terminal from the electrode pad of the solid-state image pickup device chip is provided through the metal wiring formed on a side surface or back surface of the solid-state image pickup device chip, and it can be applied to various small-size packaging where, for example, a direct mounting of chip size solid-state image pickup apparatus onto a circuit board having a signal processing circuit, etc., formed thereon is feasible.

3) In a fabricating method of solid-state image pickup apparatus having a hermetic seal portion provided over a solid-state image pickup device chip comprising a flat-plate portion formed of a transparent member and a frame portion disposed at a side portion of a lower surface of the flat plate portion, the invention according to amended claim 14 includes the steps of: over an entire wafer having a large number of solid-state image pickup device chip formed thereon, integrally and at once in a manner corresponding to each individual solid-state image pickup device chip, forming a hermetic seal portion comprising a flat-plate portion made of a transparent member, and a frame portion at least including a metal wiring disposed at a side portion of a lower surface of the flat-plate portion, a bump formed on said solid-state image pickup device chip and electrically connected to the metal wiring, and a seal region for sealing the periphery of the bump by a sealing material so that frame portion is disposed on the lower surface of the flat-plate portion where a transparent member extended over the entire wafer is used as the flat-plate portion; and separating the wafer having the hermetic seal portions formed integrally and at once thereon into solid-state image pickup device chips each having an individual hermetic seal portion.

In this manner, instead of forming the hermetic seal portions individually for each solid-state image pickup device chip on the wafer, the frame portions thereof are integrally formed collectively at once at positions corresponding to each solid-state image pickup device chip by using a transparent member which will become the flat-plate portions all over the entire wafer.

The hermetic seal portions are thereby integrally formed on all of the large number of solid-state image pickup device chips on the wafer which can be subsequently separated into individual chips to readily manufacture solid-state image pickup apparatus having a hermetic seal portion.

Concerning cited references:

The cited Nakada, on the other hand, contains a disclosure relating to image sensing device in TAB (tape automated bonding) packaging where "the lid 11 is adhered to the inner leads 5 by thermosetting of the sealant 12 after the inner leads 5 by TAB are formed on the semiconductor chip 2 through the bumps 4, thus sealing the chip surface" (column 3, lines 37 to 41). Here, the sealant 12 is applied so as to cover an end portion of the chip effective area side of the inner leads 5, thereby reducing shift in position of the lid 11 occurring at the time of thermosetting of the sealant.

The inner leads 5 connected by means of bump 4 on the semiconductor chip surface are brought out to the outside by polyimide tape 8 in TAB packaging to effect an electrical connection with an external terminal, etc.

In also cited Park, a disclosure relating to package of optical semiconductor chip such as CCD is made to achieve semiconductor package where manufacturing cost and complexity can be

reduced and at the same time a reduction in thickness is possible. Further, the package of the disclosure makes unnecessary wire bonds for connecting semiconductor chip to a circuit board in the flip chip style mounting.

In Fig. 3A to Fig. 3D of Park, a manufacturing method of semiconductor chip for adhering glass plate 20 to an upper surface of the semiconductor chip 2 is disclosed ([0062] to [0066]). According to this manufacturing method, on an upper surface of wafer W over which a large number of semiconductor chip 2 is formed, a dam 21 having a predetermined height is formed for example by a film adhesive or double-sided adhesive tape so that it is positioned at an inner side of I/O pads 2a. Subsequently, glass plate 20 is adhered to an upper surface of dam 21, and wafer W is separated into individual chips. Here, the glass plate 20 is previously formed into the size corresponding to chip 2 and is individually adhered to each chip 2 on wafer W.

Contrast between the invention of the present case and the cited references:

Claim 13 has been rejected under 35 U.S.C. 102(e) as being anticipated by Nakada. This rejection is respectfully traversed.

The Examiner then states that Nakada discloses "solid-state image pickup apparatus wherein said metal wiring is formed from an electrode pad provided on said solid-state image pickup device chip to a side surface".

The metal wiring in Nakada, however, is not formed on a side surface of solid-state image pickup device chip 2. It refers to inner leads 5 in the so-called TAB packaging, which is extended from the solid-state image pickup device chip 2 to polyimide tape 8.

Accordingly, one disclosed in Nakada is unlike the construction for making various packaging forms in chip size possible as in the invention according to claim 13 of the present case where a wiring region or an electrode pad region is formed in a manner extended through a side surface or through a side surface to a back surface of the solid-state image pickup device chip so that an external terminal can be electrically connected to the wiring region or the electrode pad region.

Further, since Nakada is of TAB packaging, it is different from chip size package according to the invention of claim 13 of the present case and, unlike the invention of the present case, is not for achieving packaging in chip size.

It is therefore believed that the solid-state image pickup apparatus according to claim 13 of the present case is totally different in construction from one disclosed in Nakada and is fully patentable.

Claim 14 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Nakada in view of Park. This rejection is respectfully traversed.

Park discloses a manufacturing method of semiconductor package where glass plate 20 is adhered to an upper surface of the semiconductor chip 2. According to this manufacturing method, glass plate 20 suitable for chip size, i.e., glass plates 20 of the size corresponding to chip 2 are individually adhered to each chip 2 on wafer W, i.e., to each of the large number of semiconductor chips 2 formed on wafer W. This is not to form glass plate collectively at once for all the chips on a wafer which is subsequently divided.

In the invention according to claim 14 of the present case, on the other hand, flat-plate portions and frame portions are formed collectively at once on a wafer with using a transparent member extended over the entire wafer as the flat-plate portions on the wafer having a large number of solid-state image pickup device chips thereon so that frame portion is disposed on a lower surface of a portion of the transparent member corresponding to the solid-state image pickup device chip formed on the wafer. The hermetic seal portions can thus be formed at once over all the solid-state image pickup device chips on the wafer. It is obviously unlike Park where each individual glass plate is adhered to each individual chip.

Accordingly, even if construction similar to solid-state image pickup apparatus having a hermetic seal portion, a premise of claim 14 of the present case, is disclosed in Nakada, manufacturing steps in the manufacturing method thereof are totally different as described above

from the manufacturing steps of Park. It is thus believed that the fabricating method of solid-state image pickup apparatus according to claim 14 of the present case is not unpatentable due to Nakada and Park, rather it is fully patentable.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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